

United States Patent [19]

Agarwal et al.

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[54] NUMERICALLY INTENSIVE COMPUTER ACCELERATOR

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[58] Field of Search 364/736, 736.03

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[57] ABSTRACT

A matrix processing unit is described which permits high speed numerical computation. The processing unit is a vector processing unit which is formed from a plurality of processing elements. The *i*th processing unit has a set of *N* registers within which the *i*th elements or words of *N* vectors of data are stored. Each processing element has an arithmetic unit which is capable of performing arithmetic operations on the *N* elements in the set of *N* registers. Each vector of data has *K* elements. Therefore, there are *K* processing elements. A vector operation of the matrix processing unit simultaneously performs the same operation on all elements of two vectors or more. A subsequent vector operation can be performed within one machine cycle time after the preceding vector operation.

16 Claims, 5 Drawing Sheets

